UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,427	01/29/2002	Jeroen Anton Johan Leijten	NL 010073	6839

24737 7590 12/02/2004

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
RIZZUTO, KEVIN P	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/059,427	LEIJTEN, JEROEN ANTON JOHAN	
	Examiner	Art Unit	
	Kevin P Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/02/04 ,5/10/02 4/22/02, 1/29/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *4 and 10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/29/02, 5/10/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Acknowledgement of papers filed: Response to restriction on 11/02/04 , IDS on 5/10/02, Oath/Declaration on 4/22/02, and original application on 1/29/02. The papers filed have been placed on record.

2. Claims 1-12 have been examined.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Europe on 1/30/2001. It is noted, however, that applicant has not filed a certified copy of the European application as required by 35 U.S.C. 119(b).

Oath/Declaration

4. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

The full name of each inventor (family name and at least one given name together with any initial) has not been set forth.

5. The oath or declaration has missing letters in the inventors typed names and addresses.

Drawings

6. The drawings are objected to because figure 2 has a misspelled label "perfetch." Also, the drawings contain multiple empty structures with only numbers as labels; this makes interpretation of the drawings difficult and confusing, specifically in figures 3 and

4. Adding descriptive names and functions of the boxes and structures in the figures will correct this issue. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Variable length VLIW instruction with instruction fetch control bits for prefetching, stalling, or realigning, in order to handle padding bits and instructions that cross cache line boundaries.

Claim Objections

8. Claims 4 and 10-12 are objected to for minor informalities.

9. As per claim 4 is objected to because of the following informalities: A misspelling of "from" in line 2, it states, "updated 'form' a position". Claim 4 is also missing a period at the end of the claim. Appropriate correction is required.

10. As per claim 10 is objected to because of the following informalities: Applicant states "said information according to a way the instructions are 'to be spread' over the memory lines." This implies the instructions are not already in the memory lines. However, figure 2 and the description of figure 2 shows the information indicating how the instructions 'are' spread over the memory lines. Examiner suggests rephrasing to claim "said information indicating the way the instructions are spread over the memory lines." Claims 11 and 12 are dependent on claim 10 and therefore are also objected to.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 10, 11 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 10 has the format of a dependent claim but in the preamble claims a computer program with an intended use for the processor of claim 1. It appears to be an independent claim, because it is not further limiting the

processor of claim 1, it is merely claiming a computer program with an intended use for that processor. The metes and bounds of this claim are not clear because it has the format of a dependent claim yet appears to be an independent claim. Claim 10 will be examined as an independent claim.

13. Applicant claims "instructions" in claim 1, line 2, and then later in claim 10, claims a computer program comprising instructions for a processor. It is unclear if the computer program comprises a different set of instructions or if they are the same set of instructions. Also, in line 2, of claim 10, applicant claims "the instructions comprising," it is unclear which instructions are being referred to, the instructions of claim 1 or the instructions of claim 10. This is further evidence of the intention for claim 10 to be an independent claim.

14. Claims 11 and 12 are dependent on claim 10 and therefore are also rejected.

Claim Rejections - 35 USC § 101

15. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

16. Claims 10-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. A computer program or code by itself and without a computer readable medium is not statutory subject matter. The only reference made to hardware is the word "processor" in the line "for a processor." This is not tangible hardware being claimed, it is intangible code intended for a processor. A

specific memory line is stated in line 11, could be a printed out line of code and therefore is also not tangible hardware. Therefore, the claims have no tangible embodiment.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 1, 6, 8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Mahin, U.S. Patent 5,644,744.

19. As per claim 1, Mahin discloses a computer system with processing unit being arranged to fetch memory lines from the memory and execute instructions from the memory lines

-Each memory line being fetched as a whole and being capable of holding more than one instruction: (Column 4, line 5-16 and column 5, lines 45-47)

-At least one instruction comprising information that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line: (The BF and T field work together to signal the processor how to control a part of processing when a boundary is crossed to a subsequent memory line. The BF bits are explained in column 6, lines 44-65.

When signaled by the BF field that a boundary is crossed, the processor will align the instructions properly. (Column 5, line 42-62))

-The processing unit being arranged to respond to the information by controlling said part as signaled by the information: (Column 5, lines 42-62)

20. As per claim 6, a computer system according to claim 1, the processing unit being a VLIW processing unit containing two or more issue slots for issuing operations from the instruction in parallel to the functional units: (Multiple (n) issue slots for simultaneous issuing (column 3, lines 62-66) are shown connecting the dispatch unit to the execute blocks 17_1 to 17_n in figure 1)

-The instructions being VLIW instructions, capable of containing two or more operations: (Each cache line fetched is 32 bytes and is capable of containing multiple operations (Column 3, lines 34-36). For example, a maximum of three 7-byte simple instructions can be fetched simultaneously (column 6, lines10-16). There is also parallel issuing (dispatching) and execution (figure 1 and column 3, lines 62-66) of operations within the cache line.

-The instruction comprising a field distinct from the operations to specify said information: (T field and BF field, column 6, lines 39-64 and figure 2)

21. As per claim 8, Mahin teaches method of processing instructions in a computer system with a processing unit and a memory,

-The processing unit being arranged to fetch memory lines from the memory and execute instructions from the memory lines capable of holding more than one instruction: (Column 4, lines 5-16)

-At least one instruction comprising information that signals explicitly how the processing unit when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line: (The BF and T field work together to signal the processor how to control a part of processing when a boundary is crossed to a subsequent memory line. The BF bits are explained in column 6, lines 44-65. When signaled by the BF field that a boundary is crossed, the processor will align the instructions properly. (Column 5, line 42-62))

-The method comprising fetching each memory line as a whole: (Column 4, lines 5-16)

-Processing an instruction from a current memory line: (Column 3, line 62 to column 4, line 2)

-Reading the information from the instruction during processing: (The BF and T fields (the information) are used to determine boundaries, therefore it is inherent that the BF and T fields are read)

-And controlling said part as signaled by the information: (The BF and T field work together to signal the processor how to control a part of processing when a boundary is crossed to a subsequent memory line. The BF bits are explained in column 6, lines 44-65. When signaled by the BF field that a boundary is crossed, the processor will align the instructions properly. (Column 5, line 42-62))

22. As per claim 10, a computer program comprising instructions for a processor according to claim 1, the instructions comprising said information according to a way the

instructions are to be spread over the memory lines: (The "T" field marks the beginning of a variable length instruction within a fetched line of code, which is an indication of the way instructions are to be spread over the memory lines. The BF fields indicate boundaries of instructions, which also is an indication of how the instructions are spread over the memory lines. (Column 4, lines 15-21 and Column 6, lines 31-64)

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 2, 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahin, U.S. Patent 5,644,744, as applied to claim 1, in view of Mohamed, U.S. Patent 6,684,319.

25. As per claim 2, Mahin teaches that the prefetched instruction is stored in anticipation buffer 51, and every time it is "emptied" it is loaded with the next sequentially anticipated cache line. Mahin does not teach that it is selectively loaded with prefetched instructions based on the information in the BF and T field. (Column 5, lines 49-62)

26. Mohamed teaches wherein information signals explicitly whether or not the subsequent memory line has to be prefetched during processing of the instruction, the

processing unit being arranged to start prefetching of the subsequent memory line in response to the information: (Column 3, lines 35-60)

27. It would have been obvious to combine the prefetch instruction flag bit of Mohamed with the processor of Mahin because of the advantages explained in Mohamed and because Mahin suggests that additional bits could be advantageous in column 6, line 66 to column 7 line 4. The prefetching of long instruction words (128 or 256 bits for example) can cause a significant amount of power to be consumed (column 1, lines 21-32 of Mohamed). Therefore, adding an additional bit for selective prefetching as taught by Mohamed would have saved power, because not every line would need to be prefetched, only those that are necessary. This advantage of using less power would have provided the motivation to add the prefetch instruction flag bit.

28. As per claim 3, a computer system according to Claim 2, wherein the information contains a prefetch bit whose value signals explicitly whether or not the subsequent memory line has to be prefetched: (The combination of Mohamed and Miller as applied to claim 2 teaches the limitations of claim 3 in Column 3, lines 35-60 of Mohamed)

29. As per claim 9, Mahin fails to teach wherein said controlling comprises at least one of causing a subsequent memory line to be prefetched or a program counter to skip to a start of the subsequent memory line or processing to be stalled when the instruction is reached as a branch target. Mahin teaches that the prefetched instruction is stored in anticipation buffer 51, and every time it is "emptied" it is loaded with the next sequentially anticipated cache line. Mahin does not teach that it is selectively loaded

with prefetched instructions based on the information in the BF and T field. (Column 5, lines 49-62)

30. Mohamed teaches wherein information signals explicitly whether or not the subsequent memory line has to be prefetched during processing of the instruction, the processing unit being arranged to start prefetching of the subsequent memory line in response to the information: (Column 3, lines 35-60)

31. It would have been obvious to combine the prefetch instruction flag bit of Mohamed with the processor of Mahin because of the advantages explained in Mohamed and because Mahin suggests that additional bits could be advantageous in column 6, line 66 to column 7 line 4. The prefetching of long instruction words (128 or 256 bits for example) can cause a significant amount of power to be consumed (column 1, lines 21-32). Therefore, adding an additional bit for selective prefetching as taught by Mohamed would have saved power, because not every line would need to be prefetched, only those that are necessary. This advantage of using less power would have provided the motivation to add the prefetch instruction flag bit. Applicant states "at least one of" in claim 9, therefore this combination of Mohamed and Mahin is sufficient to reject claim 9.

32. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mahin, U.S. Patent 5,644,744, as applied to claim 1, in view of Miller, U.S. Patent 5,819,058.

33. As per claim 4, Mahin fails to teach wherein the information signals explicitly whether or not an instruction pointer should be updated from a position behind the instruction in the current memory line to a start of the subsequent memory line, so that

information following the instruction on the current memory line is skipped over, the processing unit being arranged to update the instruction pointer to the start of the subsequent memory line in response to the information.

34. Miller teaches wherein information signals explicitly whether or not an instruction pointer should be updated from a position behind the instruction in the current memory line to a start of the subsequent memory line, so that information following the instruction on the current memory line is skipped over, the processing unit being arranged to update the instruction pointer to the start of the subsequent memory line in response to the information (Column 11, lines 35-45, Column 12, lines 10-25 and figures 7 and 8; Miller teaches that the addressing system determines that a next instruction packet has a pad instruction in front of it. It is inherent that there is information that explicitly signals the addressing system in order for the addressing system to determine there is a pad instruction, a determination couldn't be made by hardware without an explicit signal. The pad instruction is then discarded and does not cause any operation to occur in the processor, and the Aright and Aleft addresses (program counters) are incremented to point to a new memory line, therefore the pad instruction is skipped over. The Aright address points to byte 12 in memory 282 (a subsequent memory line) and Aleft points to byte 16 (a subsequent memory line) of memory 280.)

35. It would have been obvious to align variable length instructions on specific byte boundaries by adding a padding instruction, as is done in Miller, and have the explicit signal be within the instruction line in order to simplify hardware and increase the speed

of fetching. Mahin states it is desirable to fetch and dispatch multiple instructions in a cycle (Column 1, 23-24) and the invention of Mahin only fetches and dispatches one instruction at a time on the first read of a cache line. (Column 4, lines 3-14) Mahin also states that the variable length fetching hardware is extensive since instructions can start on any byte boundary. Fetching instructions that have less variance in size (a result of padding) would allow for a reduction in hardware and an increase in speed of fetching on the first read of the cache line.

36. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahin, U.S. Patent 5,644,744, as applied to claim 1, in view of Keller, U.S. Patent 6,546,478.

37. As per claims 5 and 11, Mahin failed to teach wherein the information signals explicitly whether or not processing of the instruction should be stalled, when the instruction is reached from a branching instruction, processing being stalled to fetch the subsequent memory line that contains a part of the instruction, the processing unit being arranged to stall in response to the information when the instruction is reached from the branching instruction.

38. Keller teaches information that signals (Continuation field 126 of figure 8) explicitly whether or not processing of the instruction should be stalled, when the instruction is reached from a branching instruction, processing being stalled to fetch the subsequent memory line that contains a part of the instruction, the processing unit being arranged to stall in response to the information when the instruction is reached from the branching instruction: (Column 22, lines 1-17, column 23, lines 17-24 and column 26,

line 44 to column 27, line 8; The invention of Keller uses the same PC address used to fetch instructions from the I-cache to fetch a line predictor entry 82 of figure 6 (PC shown in fig. 3). This entry contains information, including the continuation bit 126 (figure 8), which is combined with the instruction to be decoded by the decoder (fig. 4, fig. 22).

39. This information, while associated with the instruction and addressed by the same address as the instruction, is stored in a different memory than the instruction. However, examiner takes Official Notice to include a bit that contains information about the current instruction in the same memory line as the instruction itself. It would have been obvious to one of ordinary skill in the art to combine the continuation bit 126 in the instruction itself instead of in a separate line predictor entry 82 since the examiner takes Official Notice that combining a bit that contains information about the current instruction within the instruction memory line is conventional and well known. It would also have been obvious to combine the continuation bit 126 in the instruction itself instead of in a separate line predictor entry 82 since it has been held that the use of a one piece construction (instead of the two piece line predictor entry structure and I-cache disclosed in Keller) "would be merely a matter of obvious engineering choice." *In re Larson, 340 F.2d 965,968, 144 USPQ 347,349 (CCPA 1965).*

40. Adding the continuation bit to the instruction information bits that already exist would allow the processor to know whether a branch target instruction crosses a boundary in the cache and a stall should occur to fetch the next cache line. Mahin fails to teach how a cache line that needs to be fetched from memory because it is not

present in the I-cache is handled. The processor could detect the need for a memory access quickly and easily if the continuation bit was included in the cache line. The earlier a memory access is known to be needed the better because it is well known in the art that memory accesses can be costly to processing speed. Specifically in this application, the earlier the memory access is known, the earlier the instruction is fetched from memory and the earlier the instruction can be dispatched. It would have been obvious to combine the continuation bit within the cache line of Mahin because of the advantages provided above and because Mahin specifically states the advantage of being able to identify instruction boundaries through the use of tag bits in instruction lines.

41. As per claim 11, applicant states "at least one of" in line 2, therefore this combination of Keller and Mahin is sufficient to reject claim 11.

42. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mahin as applied to claims 1 and 6 above and in view of Sakhin, U.S. Patent 5,983,336.

43. As per claim 7, Mahin fails to teach that the field, in addition to said information, includes a decompression code that specifies for which issue slots the instruction contains operations. Mahin does not describe a specific issuing scheme or different types of execution units. Mahin is silent on the specifics of this area of the processor.

44. Sakhin teaches a header field (decompression code) in a VLIW instruction that specifies which issue slots the VLIW instruction contains syllables (operations) and which ones don't, in other words, which issue slots contain NOPs (Abstract, Summary,

and column 17, lines 18-29)). The NOPs are then issued to the execution units (Column 1, lines 35-42).

45. It would have been obvious to combine the decompression code (header) of Sakhin with the invention of Mahin would have allowed the scheduling of tasks to be done during compile time. This would have caused a reduction in "both the operating latency and the large and complex circuitry associated with on-chip instruction scheduling logic" (column 1, lines 23-30), which would have provided the motivation to use the decompression code.

46. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mahin and Keller as applied to claim 11, and further in view of Miller, U.S. Patent 5,819,058.

47. As per claim 12, Mahin teaches a computer program according to claim 11, comprising both a first and a second branch target instruction,

-The first branch target instruction being stored in a first memory line and being aligned to a start of the first memory line: (Mahin teaches no rules regarding aligning of branch target instructions, they are a specific type of instruction with no specific rules and therefore they are treated as any other instructions in cache memory. Therefore it is inherent that a branch instruction will be aligned at the beginning of a first memory line when the instructions line up in the appropriate manner to cause such an alignment.)

-The second branch target instruction being spread over a second and third memory line: (Mahin teaches no rules regarding aligning of branch target instructions, they are a specific type of instruction with no specific rules and therefore they are

treated as any other instructions in cache memory. Instructions in the cache memory of Mahin cross over memory line boundaries. Therefore it is inherent that a branch instruction will cross from second memory line to a third memory line when the instructions line up in the appropriate manner to cause such an alignment.)

-The second branch target instruction immediately following a preceding instruction in the second memory line (Mahin teaches Branch target instructions that can be at least 32 bytes (BTAC of figure 5, which holds a branch target instruction can hold 32 bytes). Mahin also inherently teaches that branch target instructions can cross memory line boundaries and also teaches multiple instructions on a cache line (figure 2, line B). He therefore also teaches an instruction can be immediately preceding a branch target instruction that crosses a memory boundary.

48. Mahin fails to teach:

-The explicit signal to realign being set in a preceding instruction in a preceding memory line that precedes the first memory line,

-The explicit signal to stall being cleared in the first branch target instruction;

-The explicit signal to stall being set in the second branch target instruction.

49. Miller teaches:

-A first instruction (IP4 of figure 7) being stored in a first memory line and being aligned to a start of the first memory line.

-The explicit signal to realign being set in a preceding instruction in a preceding memory line that precedes the first memory line: (Column 11, lines 35-45, Column 12, lines 10-25 and figures 7 and 8; Miller teaches that the addressing system determines

that a next instruction packet has a pad instruction in front of it. It is inherent that there is information that explicitly signals the addressing system in order for the addressing system to be able determine there is a pad instruction. The pad instruction is then discarded and does not cause any operation to occur in the processor, and the Aright and Aleft addresses (program counters) are incremented to point to a new memory line, therefore the pad instruction is skipped over. The Aright address points to byte 12 in memory 282 (a subsequent memory line) and Aleft points to byte 16 (a subsequent memory line) of memory 280. Miller also teaches that the addressing system determines that the "next instruction packet" (which requires the pc address to be incremented to be reached) has a pad instruction in front of it. Therefore, the determination of padding is made from a preceding instruction in a preceding memory line that precedes the memory line of the first instruction.

50. It would have been obvious to align variable length instructions on specific byte boundaries by adding a padding instruction, as is done in Miller, and include the explicit signal within the instruction line in order to simplify hardware and increase the speed of fetching. Mahin states it is desirable to fetch and dispatch multiple instructions in a cycle (Column 1, 23-24) and the invention of Mahin only fetches and dispatches one instruction at a time on the first read of a cache line. (Column 4, lines 3-14) Mahin also states that the variable length fetching hardware is extensive since instructions can start on any byte boundary. Fetching instructions that have less variance in size (a result of padding) would allow for a reduction in hardware and an increase in speed of fetching on the first read of the cache line.

51. The combination of Mahin and Miller fails to teach the explicit signal to stall being cleared in the first branch target instruction and the explicit signal to stall being set in the second branch target instruction.

52. Keller teaches an instruction being spread over a second and third memory line (Column 22, lines 1-17)

-The explicit signal (Continuation field 126 of figure 8) to stall being set in the second branch target instruction:(Column 22, lines 1-17, column 23, lines 17-24 and column 26, line 44 to column 27, line 8; The invention of Keller uses the same PC address used to fetch instructions from the I-cache to fetch a line predictor entry 82 of figure 6 (PC shown in fig. 3). This entry contains information, including the continuation bit 126 (figure 8), which is combined with the instruction to be decoded by the decoder (fig. 4, fig. 22). The continuation bit is set when any instruction crosses a memory line boundary that goes into another cache page, including branch target instructions.

-The explicit signal to stall being cleared in the first branch target instruction: Keller teaches that the signal to stall (continuation bit 126) is set when a boundary line is crossed. Therefore when the first branch target instruction of Mahin is aligned at the beginning of a cache line and doesn't cross a boundary line, it will be cleared.

53. This information, while associated with the instruction and addressed in the by the same address as the instruction, is stored in a different memory than the instruction. However, examiner takes Official Notice to include a bit that contains information about the current instruction in the same memory line as the instruction itself. It would have been obvious to one of ordinary skill in the art to combine the continuation bit 126 in the

instruction itself instead of in a separate line predictor entry 82 since the examiner takes Official Notice that combining a bit that contains information about the current instruction within the instruction memory line is conventional and well known. It would also have been obvious to combine the continuation bit 126 in the instruction itself instead of in a separate line predictor entry 82 since it has been held that the use of a one piece construction (instead of the two piece line predictor entry structure and I-cache disclosed in Keller) "would be merely a matter of obvious engineering choice." *In re Larson, 340 F.2d 965,968, 144 USPQ 347,349 (CCPA 1965).*

54. Adding the continuation bit to the instruction information bits that already exist would allow the processor to know whether a branch target instruction crosses a boundary in the cache and a stall should occur to fetch the next cache line. Mahin fails to teach how a cache line that needs to be fetched from memory because it is not present in the I-cache is handled. The processor could detect the need for a memory access quickly and easily if the continuation bit was included in the cache line. The earlier a memory access is known to be needed the better because it is well known in the art that memory accesses can be costly to processing speed. Specifically in this application, the earlier the memory access is known, the earlier the instruction is fetched from memory and the earlier the instruction can be dispatched. It would have been obvious to combine the continuation bit within the cache line of Mahin because of the advantages provided above and because Mahin specifically states the advantage of being able to identify instruction boundaries through the use of tags.

Conclusion

55. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571)272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571)272-4174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KPR

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100